Remarks/Arguments

Reconsideration of this application is requested.

Extension of Time

Enclosed is a request and fee for a one month extension of the period for response to the Office Action mailed on December 2, 2004. Since April 2, 2005 is a Saturday, the extended period for response expires on April 4, 2005.

Claim Status

Claims 1-22 were presented. Claims 1-4, 6-16, 19, 21 and 22 are amended, and claims 5 and 20 are canceled. Accordingly, claims 1-4, 6-19, 21 and 22 are now pending.

Claim Objections

Claims 1-22 are objected to as informal. The Action asserts that terms such as VREFn-1 would be more legible if written using parentheses or subscripts. In response, claims 1-4, 6-16, 19, 21 and 22 are amended as suggested.

Claim Rejections

Claim 1 is rejected under 35 USC 102(b) as anticipated by JP 11-97628 ("Reference 1"). Claims 2, 5-6 and 10-18 are rejected under 35 USC 103(a) as obvious over Reference 1 in view of JP 11-204740 ("Reference 2"). Claim 3 is rejected as obvious over Reference 1 in view of JP 11-312785 ("Reference 3"). Claim 4 is rejected as obvious over Reference 1 in view of Reference 2 and further in view of Reference 3. Claim 7 is rejected as obvious over Reference 1 in view of Reference 2 and further in view of JP 2000-68458 ("Reference 4"). Claims 8-9 are rejected as obvious over Reference 1 in view of Reference 2 and further in view of Reference 4 and further in view of JP 5-29464 ("Reference 5"). Claims 19-22 are rejected as obvious over Reference 1 in view of Official Notice.

In conventional semiconductor circuits, when the environment for using the circuit is known, the relationship between the external reference potential VREF and the internal reference potential $VREF_{int}$ can be provided as is appropriate for the particular environment. However, it is often impossible to determine in

advance the environment in which the semiconductor integrated circuit will be used, and thus impossible to determine the appropriate relationship between the external reference potential VREF and the internal reference potential $VREF_{int}$ for that particular environment. Once a conventional semiconductor integrated circuit is manufactured, the relationship between the external reference potential VREF and the internal reference potential $VREF_{int}$ is fixed and cannot be changed, even when the relationship is inappropriate for the environment under which the circuit is used. In Reference 1, for example, the relationship is fixed when the device is manufactured and cannot be changed when inappropriate for the environment under which the device is used.

Claims 1 and 19 are amended to recite features that overcome this significant disadvantage of prior art circuits. These features are neither shown nor suggested by any of References 1-5, taken alone or in combination. In particular, claims 1 and 19 now require:

> a storage circuit for holding data, and
>
> a control circuit for changing said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ..., $VREF_{int(n-1)}$) based on data stored in said storage circuit

These limitations correspond substantially to dependent claims 5 and 20, which are accordingly canceled.

In paragraph 13, regarding claim 5, the Action asserts that "Reference 1 does not disclose that the conversion operation of the voltage conversion circuit described in FIG. 4 is controlled based on data stored in some kind of storage means. Reference 2, on the other hand (see FIG. 4, "register 44") teaches such an apparatus. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Reference 1 with those of Reference 2, because it was common and well known in the art to control conversion

operation of a voltage conversion circuit based on data stored in a storage means." Applicant respectfully traverses this assertion.

Reference 2 discloses a semiconductor device including a register 44. However, neither Reference 1 nor Reference 2, taken alone or in combination appreciates or cures the above-discussed technical disadvantage in the manner as recited by amended claims 1 and 19. Neither of References 1 or 2 teach or suggest a control circuit for changing the relationship between the external reference potential VREF and the internal reference potential $VREF_{int}$ in accordance with necessity after the semiconductor integrated circuits have been manufactured.

Claims 2-4, 6-18, 21 and 22 depend directly or indirectly from claims 1 and 19, and are allowable for the same reasons. References 3-5 do not cure the deficiencies of References 1 and 2.

Conclusion

This application is now believed to be in condition for allowance. The Examiner is invited to call the undersigned to discuss any issues that remain after entry of this amendment. Any fees due with this response, including the extension of time fee, may be charged to our Deposit Account No. 50-1314.

Respectfully submitted,
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